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EXAMINER	
HAN, CLEMENCE S	
ART UNIT	**PAPER NUMBER**
2665	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/918,691	PRIMROSE ET AL.	
	Examiner	Art Unit	
	Clemence Han	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/15/02, 1/21/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 32, 35, 37, 38, 40 and 41 are objected to because of the following informalities: There is a typographical error in "said register interface is further coupled to said firth storage structure...". The examiner understood it as "said register interface is further coupled to said fifth storage structure...". Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claim 1-15 and 30-41 are rejected under 35 U.S.C. 102(e) as being anticipated by Watanabe (US 6,304,571).

Regarding to claim 1, Watanabe teaches a networking apparatus comprising; a switching fabric (Fig. 5, Ref 11) including a plurality of ingress/egress points (Fig. 5, Ref 15) to switch routing paths of packets received through mediums coupled to the ingress/egress points (Figure 5); a first buffering structure including

a first plurality of storage structures (Fig. 22, Ref 65) and first associated packet diversion and insertion logic (Fig. 5, Ref 22, 32), coupled to a first of said ingress/egress point to facilitate at least a selected one of diversion of selected ones of a first plurality of egress packets being routed through said first ingress/egress point onto a first one of said mediums (Fig. 5, Ref 22), and insertion of additional ones into said first plurality of egress packets being routed (Fig. 5, Ref 32); and a second buffering structure including a second plurality of storage structures (Fig. 22, Ref 65) (Even though, 65 are shown as a part of 32 in Figure 22, both 32 and 33 have the same configurations, see Column 13 Line 47-50) and second associated packet diversion and insertion logic (Fig. 5, Ref 23, 33), coupled to a second of said ingress/egress points to facilitate at least a selected one of diversion of selected ones of a second plurality of egress packets being routed through said second ingress/egress point onto a second one of said mediums (Fig. 5, Ref 23), and insertion of additional ones into said second plurality of egress packets being routed (Fig. 5, Ref 33).

Regarding to claim 2, Watanabe teaches said first buffering structure comprises a first storage structure (Fig. 22, Ref 65) to stage undiverted ones of said egress packets; a second storage structure (Fig. 23, Ref 66) to stage diverted ones of said egress packets; a divert logic (Fig. 5, Ref 22) coupled to the first

ingress/egress point and said first and second storage structures to selective route said egress packets from said first ingress/egress point (Fig. 5, Ref 15) onto a selected one of said first and second storage structures (Fig. 23, Ref 65, 66); and a register interface (Fig. 23, Ref 13), including packet unpacking logic (Fig. 23, Ref 67), coupled to the second storage structure (Fig. 23, Ref 66) to facilitate retrieval by a processor (Fig. 23, Ref 68) said diverted ones of said egress packets in unpacked portions.

Regarding to claim 3, Watanabe teaches said first buffering structure comprises a first storage structure (Fig. 22, Ref 65) coupled to the first ingress/egress point to stage undiverted ones of said egress packets; a second storage structure (Fig. 23, Ref 66) to stage insertion ones of said egress packets; a register interface (Fig. 23, Ref 13), including packet packing logic (Fig. 23, Ref 69), to facilitate provision to said second storage structure (Fig. 23, Ref 66) by a processor (Fig. 23, Ref 68) said insertion ones of said egress packets in unpacked portions; and an insertion logic (Fig. 5, Ref 32) coupled to the first and second storage structures (Fig. 23, Ref 65, 66) to selective merge said undiverted ones and said insertion ones of said egress packets.

Regarding to claim 4, Watanabe teaches said first buffering structure further

facilitates at least an additional selected one of diversion of selected ones of a first plurality of ingress packets being received from said first medium into said switching fabric through said first ingress/egress point (Fig. 5, Ref 22), and insertion of additional ones into said first plurality of ingress packets being received (Fig. 5, Ref 32).

Regarding to claim 5, Watanabe teaches said first buffering structure comprises a first storage structure (Fig. 22, Ref 65) to stage undiverted ones of said ingress packets; a second storage structure (Fig. 23, Ref 66) to stage diverted ones of said ingress packets; a divert logic (Fig. 5, Ref 22) coupled to the first medium and said first and second storage structures to selective route said ingress packets received from said first medium (Fig. 5, Ref 15) onto a selected one of said first and second storage structures (Fig. 23, Ref 65, 66); and a register interface (Fig. 23, Ref 13), including packet unpacking logic (Fig. 23, Ref 67), coupled to the second storage structure (Fig. 23, Ref 66) to facilitate retrieval by a processor (Fig. 23, Ref 68) said diverted ones of said ingress packets in unpacked portions.

Regarding to claim 6, Watanabe teaches said first buffering structure comprises a first storage structure (Fig. 22, Ref 65) coupled to the first medium to stage undiverted ones of said ingress packets; a second storage structure (Fig. 23, Ref 66) to stage insertion ones of said ingress packets; a register interface (Fig. 23,

Ref 13), including packet packing logic (Fig. 23, Ref 69), to facilitate provision to said second storage structure (Fig. 23, Ref 66) by a processor (Fig. 23, Ref 68) said insertion ones of said ingress packets in unpacked portions; and an insertion logic (Fig. 5, Ref 32) coupled to the first and second storage structures (Fig. 23, Ref 65, 66) to selective merge said undiverted ones and said insertion ones of said ingress packets.

Regarding to claim 7, Watanabe teaches said second buffering structure further facilitates at least an additional selected one of diversion of selected ones of a second plurality of ingress packets being received from said second medium into said switching fabric through said second ingress/egress point (Fig. 5, Ref 23), and insertion of additional ones into said second plurality of ingress packets being received (Fig. 5, Ref 33).

Regarding to claim 8, Watanabe teaches a networking apparatus comprising: a switching fabric (Fig. 5, Ref 11) including a plurality of ingress/egress points (Fig. 5, Ref 15) to switch routing paths of packets received through mediums coupled to the ingress/egress points (Figure 5); a first buffering structure including a first plurality of storage structures (Fig. 22, Ref 65) and first associated packet diversion and insertion logic (Fig. 5, Ref 22, 32), coupled to a first of said ingress/egress points to facilitate at least a selected one of diversion of selected

ones of a first plurality of ingress packets being received from a first one of said mediums into said switching fabric through said first ingress/egress point (Fig. 5, Ref 22), and insertion of additional ones into said first plurality of ingress packets being received (Fig. 5, Ref 32); and a second buffering structure including a second plurality of storage structures (Fig. 22, Ref 65) (Even though, 65 are shown as a part of 32 in Figure 22, both 32 and 33 have the same configurations, see Column 13 Line 47-50) and second associated packet diversion and insertion logic (Fig. 5, Ref 23, 33), coupled to a second of said ingress/egress points to facilitate at least a selected one of diversion of selected ones of a second plurality of ingress packets being received from a second one of said mediums into said switching fabric through said second ingress/egress point (Fig. 5, Ref 23), and insertion of additional ones into said second plurality of ingress packets being received (Fig. 5, Ref 33).

Regarding to claim 9, Watanabe teaches said first buffering structure comprises a first storage structure (Fig. 22, Ref 65) to stage undiverted ones of said ingress packets; a second storage structure (Fig. 23, Ref 66) to stage diverted ones of said ingress packets; a divert logic (Fig. 5, Ref 22) coupled to the first medium and said first and second storage structures to selective route said ingress packets received from said first medium (Fig. 5, Ref 15) onto a selected one of said first

and second storage structures (Fig. 23, Ref 65, 66); and a register interface (Fig. 23, Ref 13), including packet unpacking logic (Fig. 23, Ref 67), coupled to the second storage structure (Fig. 23, Ref 66) to facilitate retrieval by a processor (Fig. 23, Ref 68) said diverted ones of said ingress packets in unpacked portions.

Regarding to claim 10, Watanabe teaches said first buffering structure comprises a first storage structure (Fig. 22, Ref 65) coupled to the first medium to stage undiverted ones of said ingress packets; a second storage structure (Fig. 23, Ref 66) to stage insertion ones of said ingress packets; a register interface (Fig. 23, Ref 13) , including packet packing logic (Fig. 23, Ref 69), to facilitate provision to said second storage structure by a processor (Fig. 23, Ref 68) said insertion ones of said ingress packets in unpacked portions; and an insertion logic (Fig. 5, Ref 32) coupled to the first and second storage structures (Fig. 23, Ref 65, 66) to selective merge said undiverted ones and said insertion ones of said ingress packets.

Regarding to claim 11, Watanabe teaches a networking apparatus comprising: a switching fabric (Fig. 5, Ref 11) including a plurality of ingress/egress points (Fig. 5, Ref 15) to switch packets received through mediums coupled to the ingress/egress points (Figure 5); and a buffering structure including a first plurality of storage structures (Fig. 22, Ref 65) and first associated packet diversion and insertion logic (Fig. 5, Ref 22, 32), coupled to a first of said

ingress/egress points (Fig. 5, Ref 15), to facilitate at least a selected one of diversion of selected ones of a plurality of ingress packets being received from a first one of said mediums into said switching fabric through said first ingress/egress point (Fig. 5, Ref 22), and insertion of additional ones into said plurality of ingress packets being received (Fig. 5, Ref 32), and a second buffering structure including a second plurality of storage structures (Fig. 22, Ref 65) (Even though, 65 are shown as a part of 32 in Figure 22, both 32 and 33 have the same configurations, see Column 13 Line 47-50) and second associated packet diversion and insertion logic (Fig. 5, Ref 23, 33), coupled to the first ingress/egress point (Fig. 5, Ref 15), to facilitate at least a selected one of diversion of selected ones of a plurality of egress packets being routed through said first ingress/egress point onto said first medium (Fig. 5, Ref 23), and insertion of additional ones into said plurality of ingress packets being routed (Fig. 5, Ref 33).

Regarding to claim 12, Watanabe teaches said first plurality of storage structures and associated first packet diversion and insertion logic comprises a first storage structure (Fig. 22, Ref 65) to stage undiverted ones of said egress packets; a second storage structure (Fig. 23, Ref 66) to stage diverted ones of said egress packets; a dived logic (Fig. 5, Ref 22) coupled to the first ingress/egress point and said first and second storage structures to selective route said egress packets from

said first ingress/egress point (Fig. 5, Ref 15) onto a selected one of said first and second storage structures (Fig. 23, Ref 65, 66); and a register interface (Fig. 23, Ref 13), including packet unpacking logic (Fig. 23, Ref 67), coupled to the second storage structure (Fig. 23, Ref 66) to facilitate retrieval by a processor (Fig. 23, Ref 68) said diverted ones of said egress packets in unpacked portions.

Regarding to claim 13, Watanabe teaches said first plurality of storage structures and associated first packet diversion and insertion logic comprises a first storage structure (Fig. 22, Ref 65) coupled to the first ingress/egress point to stage undiverted ones of said egress packets; a second storage structure (Fig. 23; Ref 66) to stage insertion ones of said egress packets; a register interface (Fig. 23, Ref 13), including packet packing logic (Fig. 23, Ref 69), to facilitate provision to said second storage structure (Fig. 23, Ref 66) by a processor (Fig. 23, Ref 68) said insertion ones of said egress packets in unpacked portions; and an insertion logic (Fig. 5, Ref 32) coupled to the first and second storage structures (Fig. 23, Ref 65, 66) to selective merge said undiverted ones and said insertion ones of said egress packets.

Regarding to claim 14, Watanabe teaches said second plurality of storage structures and associated second packet diversion and insertion logic comprises a first storage structure (Fig. 22, Ref 65) (Even though, 65 are shown as a part of 32

in Figure 22, both 32 and 33 have the same configurations, see Column 13 Line 47-50) to stage undiverted ones of said ingress packets; a second storage structure (Fig. 23, Ref 66) (Even though, 66 are shown as a part of said first buffering structure in Figure 23, both buffering structures have the same configurations, see Column 13 Line 53-62) to stage diverted ones of said ingress packets; a divert logic (Fig. 5, Ref 23) coupled to the first medium and said first and second storage structures (Fig. 23, Ref 65, 66) to selective route said ingress packets received from said first medium onto a selected one of said first and second storage structures; and a register interface (Fig. 23, Ref 13), including packet unpacking logic (Fig. 23, Ref 67) (Even though, 67 are shown as a part of said first buffering structure in Figure 23, both buffering structures have the same configurations, see Column 13 Line 53-62), coupled to the second storage structure (Fig. 23, Ref 66) to facilitate retrieval by a processor (Fig. 23, Ref 68) said diverted ones of said ingress packets in unpacked portions.

Regarding to claim 15, Watanabe teaches said second plurality of storage structures and associated second packet diversion and insertion logic comprises a first storage structure (Fig. 22, Ref 65) (Even though, 65 are shown as a part of 32 in Figure 22, both 32 and 33 have the same configurations, see Column 13 Line 47-50) coupled to the first medium to stage undiverted ones of said ingress

packets; a second storage structure (Fig. 23, Ref 66) (Even though, 66 are shown as a part of said first buffering structure in Figure 23, both buffering structures have the same configurations, see Column 13 Line 53-62) to stage insertion ones of said ingress packets; a register interface (Fig. 23, Ref 13), including packet packing logic (Fig. 23, Ref 69) (Even though, 69 are shown as a part of said first buffering structure in Figure 23, both buffering structures have the same configurations, see Column 13 Line 53-62), to facilitate provision to said second storage structure (Fig. 23, Ref 66) by a processor (Fig. 23, Ref 68) said insertion ones of said ingress packets in unpacked portions; and an insertion logic (Fig. 5, Ref 33) coupled to the first and second storage structures (Fig. 23, Ref 65, 66) to selective merge said undiverted ones and said insertion ones of said ingress packets.

Regarding to claim 30, Watanabe teaches a buffering structure comprising: a first storage structure (Fig. 22, Ref 65) to stage undiverted ones of egress packets; a second storage structure (Fig. 23, Ref 66) to stage diverted ones of egress packets; a third storage structure (Fig. 23, Ref 66) to stage insertion ones of egress packets; a first divert logic (Fig. 5, Ref 22) coupled to said first and second storage structures (Fig. 23, Ref 65, 66) to selectively route egress packets onto a selected one of said first and second storage structures; a first insert logic (Fig. 5, Ref 32) coupled to said first and third storage structures (Fig. 23, Ref 65, 66) to selectively

merge said undiverted ones and said insertion ones of said egress packets; and a register interface (Fig. 23, Ref 13), including packet packing and unpacking logic (Fig. 23, Ref 67, 69), coupled to the second and third storage structures (Fig. 23, Ref 66) to facilitate retrieval by a processor (Fig. 23, Ref 68) said diverted ones of said egress packets in unpacked portions, and provision by said processor said insertion ones of said egress packets in unpacked portions.

Regarding to claim 31, Watanabe teaches said buffering structure further comprises a fourth storage structure (Fig. 22, Ref 65) (Even though, 65 are shown as a part of 32 in Figure 22, both 32 and 33 have the same configurations, see Column 13 Line 47-50) to stage undiverted ones of ingress packets; a fifth storage structure (Fig. 23, Ref 66) (Even though, 66 are shown as a part of said first buffering structure in Figure 23, both buffering structures have the same configurations, see Column 13 Line 53-62) to stage diverted ones of ingress packets; a second divert logic (Fig. 5, Ref 23) coupled to said fourth and fifth storage structures (Fig. 23, Ref 65, 66) to selective route ingress packets onto a selected one of said fourth and fifth storage structures, and said register interface (Fig. 23, Ref 13), also coupled to the fifth storage structure (Fig. 23, Ref 66) to facilitate retrieval by said processor (Fig. 23, Ref 68) said diverted ones of said ingress packets in unpacked portions.

Regarding to claim 32, Watanabe teaches said buffering structure further comprises a fourth storage structure (Fig. 22, Ref 65) (Even though, 65 are shown as a part of 32 in Figure 22, both 32 and 33 have the same configurations, see Column 13 Line 47-50) to stage undiverted ones of ingress packets, a fifth storage structure (Fig. 23, Ref 66) (Even though, 66 are shown as a part of said first buffering structure in Figure 23, both buffering structures have the same configurations, see Column 13 Line 53-62) to stage insertion ones of ingress packets, and an insertion logic (Fig. 5, Ref 33) coupled to the fourth and fifth storage structures (Fig. 23, Ref 65, 66) to selective merge said undiverted ones and said insertion ones of said ingress packets; and said register interface (Fig. 23, Ref 13) is further coupled to said fifth storage structures (Fig. 23, Ref 66) to facilitate provision to said fifth storage structure by said processor (Fig. 23, Ref 68) said insertion ones of said ingress packets in unpacked portions.

Regarding to claim 33, Watanabe teaches a buffering structure comprising: a first storage structure (Fig. 22, Ref 65) to stage undiverted ones of ingress packets; a second storage structure (Fig. 23, Ref 66) to stage diverted ones of ingress packets; a third storage structure (Fig. 23, Ref 66) to stage insertion ones of ingress packets; a first divert logic (Fig. 5, Ref 22) coupled to said first and second storage structures (Fig. 23, Ref 65, 66) to selectively route ingress packets onto a

selected one of said first and second storage structures; a first insert logic (Fig. 5, Ref 32) coupled to said first and third storage structures (Fig. 23, Ref 65, 66) to selectively merge said undiverted ones and said insertion ones of said ingress packets; and a register interface (Fig. 23, Ref 13), including packet packing and unpacking logic (Fig. 23, Ref 67, 69), coupled to the second and third storage structures (Fig. 23, Ref 66) to facilitate retrieval by a processor (Fig. 23, Ref 68) said diverted ones of said ingress packets in unpacked portions, and provision by said processor said insertion ones of said ingress packets in unpacked portions.

Regarding to claim 34, Watanabe teaches said buffering structure further comprises a fourth storage structure (Fig. 22, Ref 65) (Even though, 65 are shown as a part of 32 in Figure 22, both 32 and 33 have the same configurations, see Column 13 Line 47-50) to stage undiverted ones of egress packets; a fifth storage structure (Fig. 23, Ref 66) (Even though, 66 are shown as a part of said first buffering structure in Figure 23, both buffering structures have the same configurations, see Column 13 Line 53-62) to stage diverted ones of egress packets; a second dived logic (Fig. 5, Ref 23) coupled to said fourth and fifth storage structures (Fig. 23, Ref 65, 66) to selective route egress packets onto a selected one of said fourth and fifth storage structures; and said register interface (Fig. 23, Ref 13), also coupled to the fifth storage structure (Fig. 23, Ref 66) to

facilitate retrieval by said processor (Fig. 23, Ref 68) said diverted ones of said egress packets in unpacked portions.

Regarding to claim 35, Watanabe teaches said buffering structure further comprises a fourth storage structure (Fig. 22, Ref 65) (Even though, 65 are shown as a part of 32 in Figure 22, both 32 and 33 have the same configurations, see Column 13 Line 47-50) to stage undiverted ones of egress packets, a fifth storage structure (Fig. 23, Ref 66) (Even though, 66 are shown as a part of said first buffering structure in Figure 23, both buffering structures have the same configurations, see Column 13 Line 53-62) to stage insertion ones of egress packets, and an insertion logic (Fig. 5, Ref 33) coupled to the fourth and fifth storage structures (Fig. 23, Ref 65, 66) to selective merge said undiverted ones and said insertion ones of said egress packets; and said register interface (Fig. 23, Ref 13) is further coupled to said fifth storage structures (Fig. 23, Ref 66) to facilitate provision to said fifth storage structure by said processor (Fig. 23, Ref 68) said insertion ones of said egress packets in unpacked portions.

Regarding to claim 36, Watanabe teaches a buffering structure comprising: a first storage structure (Fig. 22, Ref 65) to stage undiverted ones of ingress packets, a second storage structure (Fig. 23, Ref 66) to stage diverted ones of ingress packets; a third storage structure (Fig. 22, Ref 65) (Even though, 65 are

shown as a part of 32 in Figure 22, both 32 and 33 have the same configurations, see Column 13 Line 47-50) to stage undiverted ones of egress packets; a fourth storage structure (Fig. 23, Ref 66) (Even though, 66 are shown as a part of said first buffering structure in Figure 23, both buffering structures have the same configurations, see Column 13 Line 53-62) to stage diverted ones of egress packets; a first divert logic (Fig. 5, Ref 22) coupled to said first and second storage structures (Fig. 23, Ref 65, 66) to selectively route ingress packets onto a selected one of said first and second storage structures; a second divert logic (Fig. 5, Ref 23) coupled to said third and fourth storage structures (Fig. 23, Ref 65, 66) (see Column 13 Line 47-50 and Line 53-62) to selectively route egress packets onto a selected one of said third and fourth storage structures; and a register interface (Fig. 23, Ref 13), including packet unpacking logic (Fig. 23, Ref 67) (Even though, 67 are shown as a part of said first buffering structure in Figure 23, both buffering structures have the same configurations, see Column 13 Line 53-62), coupled to the second and fourth storage structures (Fig. 23, Ref 66) to facilitate retrieval by a processor (Fig. 23, Ref 68) said diverted ones of said ingress and egress packets in unpacked portions.

Regarding to claim 37, Watanabe teaches said buffering structure further comprises a fifth storage structure (Fig. 23, Ref 66) to stage insertion ones of

ingress packets, an insertion logic (Fig. 5, Ref 32) coupled to the first and fifth storage structures (Fig. 23, Ref 65, 66) to selective merge said undiverted ones and said insertion ones of said ingress packets; and said register interface (Fig. 23, Ref 13) is further coupled to said fifth storage structures (Fig. 23, Ref 66) to facilitate provision to said fifth storage structure by said processor (Fig. 23, Ref 68) said insertion ones of said ingress packets in unpacked portions.

Regarding to claim 38, Watanabe teaches said buffering structure further comprises a fifth storage structure (Fig. 23, Ref 66) to stage insertion ones of egress packets, and an insertion logic (Fig. 5, Ref 33) coupled to the third and fifth storage structures (Fig. 23, Ref 65, 66) (see Column 13 Line 47-50 and Line 53-62) to selective merge said undiverted ones and said insertion ones of said egress packets; and said register interface (Fig. 23, Ref 13) is further coupled to said fifth storage structures (Fig. 23, Ref 66) to facilitate provision to said fifth storage structure by said processor (Fig. 23, Ref 68) said insertion ones of said egress packets in unpacked portions.

Regarding to claim 39, Watanabe teaches a buffering structure comprising: a first storage structure (Fig. 22, Ref 65) to stage undiverted ones of ingress packets; a second storage structure (Fig. 23, Ref 66) to stage insertion ones of ingress packets; a third storage structure (Fig. 22, Ref 65) (Even though, 65 are

shown as a part of 32 in Figure 22, both 32 and 33 have the same configurations, see Column 13 Line 47-50) to stage undiverted ones of egress packets; a fourth storage structure (Fig. 23, Ref 66) (Even though, 66 are shown as a part of said first buffering structure in Figure 23, both buffering structures have the same configurations, see Column 13 Line 53-62) to stage insertion ones of egress packets; a first insertion logic (Fig. 5, Ref 32) coupled to the first and second storage structures (Fig. 23, Ref 65, 66) to selective merge said undiverted ones and said insertion ones of said ingress packets; a second insertion logic (Fig. 5, Ref 33) coupled to the third and fourth storage structures (Fig. 23, Ref 65, 66) (see Column 13 Line 47-50 and Line 53-62) to selective merge said undiverted ones and said insertion ones of said egress packets; and a register interface (Fig. 23, Ref 13), including packet packing logic (Fig. 23, Ref 69) (Even though, 69 are shown as a part of said first buffering structure in Figure 23, both buffering structures have the same configurations, see Column 13 Line 53-62), coupled to the second and fourth storage structures (Fig. 23, Ref 66) to facilitate provision by a processor (Fig. 23, Ref 68) said insertion ones of said ingress and egress packets in unpacked portions.

Regarding to claim 40, Watanabe teaches said buffering structure further comprises a fifth storage structure (Fig. 23, Ref 66) to stage diverted ones of ingress packets, a divert logic (Fig. 5, Ref 22) coupled to the first and fifth storage

structures (Fig. 23, Ref 65, 66) to selectively route ingress packets onto a selected one of said first and fifth storage structures; and said register interface (Fig. 23, Ref 13) is further coupled to said fifth storage structures (Fig. 23, Ref 66) to facilitate retrieval by said processor (Fig. 23, Ref 68) said diverted ones of said ingress packets in unpacked portions.

Regarding to claim 41, Watanabe teaches said buffering structure further comprises a fifth storage structure (Fig. 23, Ref 66) to stage diverted ones of egress packets, a divert logic (Fig. 5, Ref 23) coupled to the third and fifth storage structures (Fig. 23, Ref 65, 66) (see Column 13 Line 47-50 and Line 53-62) to selectively route egress packets onto a selected one of said third and fifth storage structures; and said register interface (Fig. 23, Ref 13) is further coupled to said fifth storage structures (Fig. 23, Ref 66) to facilitate retrieval by said processor (Fig. 23, Ref 68) said diverted ones of said egress packets in unpacked portions.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 16-20, 22-27 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe in view of Baydar et al. (US 6,049,550).

Regarding to claim 16, Watanabe teaches a networking module comprising; a data link/physical layer processing unit, including a buffering structure comprising a plurality of storage structures (Fig. 22, Ref 65) and associated packet diversion and insertion logic (Fig. 5, Ref 22, 32) to facilitate at least a selected one of data link/physical processing of ingress packets received from a medium for said packet source/sink and egress packets to be routed from said packet source/sink onto said medium, with each of said data link/physical processing of ingress and egress packets including at least a selected one of diversion of selected ones of a plurality of ingress/egress packets being received from/routed onto said medium (Fig. 5, Ref 22), and insertion of additional ones into said plurality of ingress/egress packets being received/routed (Fig. 5, Ref 32). Watanabe, however, does not teach an optical component to send and receive optical signals encoded with data transmitted through a coupled optical medium; an optical-electrical component coupled to the optical component to encode digital data onto optical signals and to decode encoded digital data on optical signals back into their digital forms; a data link/physical layer processing unit coupled to the optical-electrical component and to a packet source/sink; and a body encasing said optical

component, said optical-electrical component, and said data link/physical processing unit as a single module. Baydar teaches an optical component (Fig. 29, Ref 265, 271) to send and receive optical signals encoded with data transmitted through a coupled optical medium; an optical-electrical component (Fig. 29, Ref 60) coupled to the optical component to encode digital data onto optical signals and to decode encoded digital data on optical signals back into their digital forms; a data link/physical layer processing unit (Fig. 29, Ref 274) coupled to the optical-electrical component (Fig. 29, Ref 265, 271) and to a packet source/sink (Fig. 29, Ref 267, 269); and a body encasing said optical component, said optical-electrical component, and said data link/physical processing unit as a single module (Figure 29, Column 44). It would have been obvious to one skilled in the art to modify Watanabe to be used in optical environment as taught by Baydar in order to be able to interface with switch systems of the future, as well as those presently in service, including analog and digital system (Column 1 Line 24-53).

Regarding to claim 17, Watanabe teaches said plurality of storage structures and associated packet diversion and insertion logic comprises a first storage structure (Fig. 22, Ref 65) to stage undiverted ones of said egress packets; a second storage structure (Fig. 23, Ref 66) to stage diverted ones of said egress packets; a divert logic (Fig. 5, Ref 22) coupled to said packet source/sink and said first and

second storage structures to selectively route said egress packets from said packet source/sink onto a selected one of said first and second storage structures (Fig. 23, Ref 65, 66); and a register interface (Fig. 23, Ref 13), including packet unpacking logic (Fig. 23, Ref 67), coupled to the second storage structure (Fig. 23, Ref 66) to facilitate retrieval by a processor (Fig. 23, Ref 68) said diverted ones of said egress packets in unpacked portions.

Regarding to claim 18, Watanabe teaches said plurality of storage structures and associated packet diversion and insertion logic comprises a first storage structure (Fig. 22, Ref 65) coupled to the packet source/sink to stage undiverted ones of said egress packets; a second storage structure (Fig. 23, Ref 66) to stage insertion ones of said egress packets; a register interface (Fig. 23, Ref 13), including packet packing logic (Fig. 23, Ref 69), to facilitate provision to said second storage structure (Fig. 23, Ref 66) by a processor (Fig. 23, Ref 68) said insertion ones of said egress packets in unpacked portions; and an insertion logic coupled to the first and second storage structures (Fig. 23, Ref 65, 66) to selective merge said undiverted ones and said insertion ones of said egress packets.

Regarding to claim 19, Watanabe teaches said plurality of storage structures and associated packet diversion and insertion logic comprises a first storage structure (Fig. 22, Ref 65) to stage undiverted ones of said ingress packets; a

second storage structure (Fig. 23, Ref 66) to stage diverted ones of said ingress packets; a divert logic (Fig. 5, Ref 22) coupled to the medium and said first and second storage structures (Fig. 23, Ref 65, 66) to selective route said ingress packets received from said medium onto a selected one of said first and second storage structures; and a register interface (Fig. 23, Ref 13), including packet unpacking logic (Fig. 23, Ref 67), coupled to the second storage structure (Fig. 23, Ref 66) to facilitate retrieval by a processor (Fig. 23, Ref 68) said diverted ones of said ingress packets in unpacked portions.

Regarding to claim 20, Watanabe teaches said plurality of storage structures and associated packet diversion and insertion logic comprises a first storage structure (Fig. 22, Ref 65) coupled to the medium to stage undiverted ones of said ingress packets; a second storage structure (Fig. 23, Ref 66) to stage insertion ones of said ingress packets; a register interface (Fig. 23, Ref 13), including packet packing logic (Fig. 23, Ref 69), to facilitate provision to said second storage structure (Fig. 23, Ref 66) by a processor (Fig. 23, Ref 68) said insertion ones of said ingress packets in unpacked portions; and an insertion logic (Fig. 5, Ref 32) coupled to the first and second storage structures (Fig. 23, Ref 65, 66) to selective merge said undiverted ones and said insertion ones of said ingress packets.

Regarding to claim 22, Watanabe teaches said data link/physical layer processing unit is a multi-protocol processor that supports a plurality of datacom and telecom protocols (Column 5 Line 13-21).

Regarding to claim 23, Watanabe teaches a multi-protocol processor comprising: a plurality of I/O interfaces to facilitate selective trafficking of data transmitted in accordance with a selected one of a plurality of datacom and telecom protocols (Figure 1); a plurality of data link and physical sub-layer processing units 12 selectively coupled to each other and to the I/O interfaces (Fig. 5, Ref 15) to be selectively employed in combination to perform selected data link and physical sub-layer processing on egress as well as ingress ones of said data, in accordance with said selected one of said plurality of protocols; and a buffering structure coupled to at least a system-side one of said I/O interfaces and a media processing one of said data link and physical sub-layer processing units, including a plurality of storage structures (Fig. 22, Ref 65) and associated packet diversion and insertion logic (Fig. 5, Ref 22, 32) to facilitate at least a selected one of diversion of selected ones of a plurality of egress packets (Fig. 5, Ref 22), and insertion of additional ones into said plurality of egress packets (Fig. 5, Ref 32), diversion of selected ones of a plurality of ingress packets (Fig. 5, Ref 23), and insertion of additional ones into said plurality of ingress packets (Fig. 5, Ref 33). Watanabe, however,

does not teach I/O interfaces to facilitate selective optical-electrical trafficking of data. Baydar teaches I/O interfaces to facilitate selective optical-electrical trafficking of data (Fig. 29, Ref 60) (Figure 29, Column 44). It would have been obvious to one skilled in the art to modify Watanabe to be used in optical environment as taught by Baydar in order to be able to interface with switch systems of the future, as well as those presently in service, including analog and digital system (Column 1 Line 24-53).

Regarding to claim 24, Watanabe teaches said plurality of storage structures and associated packet diversion and insertion logic comprises a first storage structure (Fig. 22, Ref 65) to stage undiverted ones of said egress packets; a second storage structure (Fig. 23, Ref 66) to stage diverted ones of said egress packets; a divert logic (Fig. 5, Ref 22) coupled to said packet source/sink and said first and second storage structures to selectively route said egress packets from said packet source/sink onto a selected one of said first and second storage structures (Fig. 23, Ref 65, 66); and a register interface (Fig. 23, Ref 13), including packet unpacking logic (Fig. 23, Ref 67), coupled to the second storage structure (Fig. 23, Ref 66) to facilitate retrieval by a processor (Fig. 23, Ref 68) said diverted ones of said egress packets in unpacked portions.

Regarding to claim 25, Watanabe teaches said plurality of storage structures and associated packet diversion and insertion logic comprises a first storage structure (Fig. 22, Ref 65) coupled to the packet source/sink to stage undiverted ones of said egress packets; a second storage structure (Fig. 23, Ref 66) to stage insertion ones of said egress packets; a register interface (Fig. 23, Ref 13), including packet packing logic (Fig. 23, Ref 69), to facilitate provision to said second storage structure (Fig. 23, Ref 66) by a processor (Fig. 23, Ref 68) said insertion ones of said egress packets in unpacked portions; and an insertion logic coupled to the first and second storage structures (Fig. 23, Ref 65, 66) to selective merge said undiverted ones and said insertion ones of said egress packets.

Regarding to claim 26, Watanabe teaches said plurality of storage structures and associated packet diversion and insertion logic comprises a first storage structure (Fig. 22, Ref 65) to stage undiverted ones of said ingress packets; a second storage structure (Fig. 23, Ref 66) to stage diverted ones of said ingress packets; a divert logic (Fig. 5, Ref 22) coupled to the medium and said first and second storage structures (Fig. 23, Ref 65, 66) to selective route said ingress packets received from said medium onto a selected one of said first and second storage structures; and a register interface (Fig. 23, Ref 13), including packet unpacking logic (Fig. 23, Ref 67), coupled to the second storage structure (Fig. 23,

Ref 66) to facilitate retrieval by a processor (Fig. 23, Ref 68) said diverted ones of said ingress packets in unpacked portions.

Regarding to claim 27, Watanabe teaches said plurality of storage structures and associated packet diversion and insertion logic comprises a first storage structure (Fig. 22, Ref 65) coupled to the optical medium to stage undiverted ones of said ingress packets; a second storage structure (Fig. 23, Ref 66) to stage insertion ones of said ingress packets; a register interface (Fig. 23, Ref 13), including packet packing logic (Fig. 23, Ref 69), to facilitate provision to said second storage structure (Fig. 23, Ref 66) by a processor (Fig. 23, Ref 68) said insertion ones of said ingress packets in unpacked portions; and an insertion logic coupled to the first and second storage structures (Fig. 23, Ref 65, 66) to selective merge said undiverted ones and said insertion ones of said ingress packets.

Regarding to claim 29, Watanabe teaches said processor is disposed on a single integrated circuit (Fig. 5, Ref 12).

6. Claim 21 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe in view of Baydar et al. and further in view of Jannson et al. (US Pub. 2003/0081287).

Regarding to claim 21, Watanabe teaches said data link/physical layer processing unit are all designed to support data rates of at least 600 Mbps (Column

3 Line 53-54). Baydar teaches said optical and optical-electrical components, said data link/physical layer processing unit are all designed to support data rates of at least 622.08 Mbps (Column 1 Line 53). Watanabe in view of Baydar, however, does not teach said optical and optical-electrical components, said data link/physical layer processing unit are all designed to support data rates of at least 10GB/s. Jannson teaches said optical and optical-electrical components, said data link/physical layer processing unit are all designed to support data rates of at least 10GB/s [0026]. It would have been obvious to one skilled in the art to modify Watanabe in view of Baydar to support 10GB/s as taught by Jannson in order to meet the demand for high capacity communication links [0004].

Regarding to claim 28, Watanabe teaches said data link/physical layer processing unit are all designed to support data rates of at least 600 Mbps (Column 3 Line 53-54). Baydar teaches said optical and optical-electrical components, said data link/physical layer processing unit are all designed to support data rates of at least 622.08 Mbps (Column 1 Line 53). Watanabe in view of Baydar, however, does not teach said optical and optical-electrical components, said data link/physical layer processing unit are all designed to support data rates of at least 10GB/s. Jannson teaches said optical and optical-electrical components, said data link/physical layer processing unit are all designed to support data rates of at least

10GB/s [0026]. It would have been obvious to one skilled in the art to modify Watanabe in view of Baydar to support 10GB/s as taught by Jannson in order to meet the demand for high capacity communication links [0004].

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents are cited to further show the state of the art with respect to the invention in general.

U.S. Patent 5,613,069 to Walker

U.S. Patent 6,792,174 to Ramaswami

U.S. Pub. 2002/0122386 to Calvignac et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clemence Han whose telephone number is (571) 272-3158. The examiner can normally be reached on Monday-Thursday 7 - 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C. H.

Clemence Han
Examiner
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STEVEN NGUYEN
PRIMARY EXAMINER